Simplification in a satisfiability checker for VLSI applications. (English) Zbl 0783.94031

Summary: INSTEP is a satisfiability checker designed for the original purpose of solving a specific target set of problems in the formal verification of VLSI circuits. These are real-world problems concerning a sequential circuit that is part of a commercial chip manufactured by Texas Instruments. The program has succeeded in solving these problems, which require satisfiability checking for combinational representations containing up to around 10000 variables and a graphical representation of around 17000 nodes. It has also been successfully applied to a number of standard benchmark problems in combinational circuit verification. Results on these benchmarks are overall competitive with those for the widely used method based on binary decision diagrams, and for the first time demonstrate the solution in polynomial time of certain benchmarks involving combinational multipliers.

A central part of the INSTEP algorithm is simplification. Most simplifications that take place in previous tautology checkers consist of the replacement of a formula by a shorter formula that is logically equivalent. Most simplifications in INSTEP replace a formula by another formula which is not logically equivalent, but such that satisfiability is nevertheless preserved. These new simplifications depend on the pattern of occurrence of one or more variables and particularly on their polarity.

The simplifications used by INSTEP rest on several new theorems in an area of propositional calculus (or Boolean algebra) which is crucial to the general theory of effective simplification of propositional formulas. The primary purpose of the paper is to demonstrate these theorems and explain the simplifications that depend on them.

We have tried INSTEP on the well-known pigeonhole problem. So far as we know INSTEP is the first implemented program to produce proofs of polynomial length for pigeonhole problems. It is also produces these proofs in polynomial time.

MSC:
94C12 Fault detection; testing in circuits and networks
68Q60 Specification and verification (program logics, model checking, etc.)

Keywords:
satisfiability checker; formal verification of VLSI circuits; combinational circuit verification; simplification; pigeonhole problem

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References:

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