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Safe reasoning with Logic LTS. (English) Zbl 1206.68189

Summary: Previous work has introduced the setting of Logic LTS, together with a variant of ready simulation as fully-abstract refinement preorder, which allows one to compose operational specifications using a CSP-style parallel operator as well as the propositional connectives conjunction and disjunction. In this paper, we show how a temporal logic for specifying safety properties may be embedded into Logic LTS so that (a) the temporal operators are compositional for ready simulation and (b) ready simulation, when restricted to pairs of processes and formulas, coincides with the logic’s satisfaction relation. The utility of this setting as a semantic foundation for mixed operational and temporal-logic specification languages is demonstrated via a simple example.

MSC:
68Q60 Specification and verification (program logics, model checking, etc.)
03B44 Temporal logic

Full Text: DOI

References:


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