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Correct hardware synthesis. (English) Zbl 1234.68067

Summary: This paper presents an algebraic compilation approach to the correct synthesis (compilation into hardware) of a synchronous language with shared variables and parallelism. The synthesis process generates a hardware component that implements the source program by means of gradually reducing it into a highly parallel state-machine. The correctness of the compiler follows by construction from the correctness of the transformations involved in the synthesis process. Each transformation is proved sound from more basic algebraic laws of the source language; the laws are themselves formally derived from a denotational semantics expressed in the unified theories of programming. The proposed approach is based on previous efforts that handle both software and hardware compilation, in a pure algebraic style, but the complexity of our source language demanded significant adaptations and extensions to the existing approaches.

MSC:
68N20 Theory of compilers and interpreters
68N15 Theory of programming languages
68Q60 Specification and verification (program logics, model checking, etc.)

Software:
Z

Full Text: DOI

References:

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